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Application Number 10/590067
Response to Office Action dated 6/27/2008

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor wafer polishing pad comprising a polishing layer and a cushion layer, wherein the polishing layer is formed from foamed polyurethane and has a flexural modulus of 250 to 350 MPa, and the cushion layer is formed from closed-cell foam and has a thickness of 0.5 to 1.0 mm and a strain constant of 0.01 to 0.08 μm/(gf/cm^2).

2. (Original) The polishing pad according to Claim 1, wherein the foamed polyurethane has an average cell diameter of 1 to 70 μm.

3. (Previously Presented) The polishing pad according to Claim 1, wherein the foamed polyurethane has a specific gravity of 0.5 to 1.0 g/cm^3.

4. (Previously Presented) The polishing pad according to Claim 1, wherein the foamed polyurethane has a Shore D hardness of 45 to 65.

5. (Previously Presented) The polishing pad according to Claim 1, wherein the foamed polyurethane has a compressibility of 0.5 to 5.0%.

6. (Previously Presented) The polishing pad according to Claim 1, wherein the cushion layer is formed from at least one material selected from the group consisting of polyurethane resin and polyethylene resin.

7. (Previously Presented) A method of producing a semiconductor device comprising at least a step of polishing a surface of a semiconductor wafer by using the polishing pad according to Claim 1.